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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
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ART UNIT	PAPER NUMBER
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/678,609	HONDA, HIROKAZU
	Examiner	Art Unit
	David E Graybill	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43,45-59 and 80-85* is/are pending in the application.

4a) Of the above claim(s) *22-26 and 55-59* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21,27-43,45-54 and 80-85* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ___ _ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5-12-3 has been entered.

Claims 22-26 and 55-59 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the outstanding response.

To further afford applicant the benefit of compact prosecution, the restriction requirement between the species wherein the plate is made of metal and ceramic is herein withdrawn, and the claims readable on those species are examined on their merits.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the rigidity limitations of the claims must be shown or the features canceled from the claims. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-21, 27-43, 45-54 and 80-85 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1, 8, 80 and 82 the limitations that the plate is securely fixed to and directly in contact with the board, and the plate being higher in rigidity than the board, appear to be incompatible because it appears that the plate and the board would have the same rigidity as the combination of the plate and the board.

In claims 1, 3, 5, 8, 10, 12 and 80-85 the scope of the term "rigidity" is unclear because the term appears to be given a meaning repugnant to its usual meaning of the quality or state of being deficient in or devoid of flexibility, or the quality or state of having the outer shape maintained by a fixed framework.

In claim 15 the limitation wherein the chip is bonded via bumps to the second surface, and in claim 16 the limitation wherein resin material is provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps, appears to be incompatible with the claim 8 limitation wherein the chip is mounted on the first surface.

In claims 18, 27, 29, 32, 36, 37 and 42 the word "means" is preceded by the words "buffer layer" in an attempt to use a means clause to recite a claim element as a means for performing a specified function. However, since no function is specified by the words preceding "means," it is impossible to determine the equivalents of the element, as required by 35 U.S.C. 112, sixth paragraph. See *Ex parte Klumb*, 159 USPQ 694 (Bd. App. 1967). To further clarify, if "buffer layer means" is restated as "means for buffer layering," the phrase makes no sense because the term "buffer layering" has no functional connotation, and the phrase is indefinite.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-21, 27-43, 45-54 and 80-85 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

The claims contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The undescribed subject matter is the term "rigidity." In particular, one skilled in the art would not be able to make or use the claimed product having the quality or state of being deficient in or devoid of flexibility, or

having the quality or state of having the outer shape maintained by a fixed framework, because the specification contains no clear standard for measuring this quality. Furthermore, the structure imparted to the product by the term *rigidity* cannot be determined.

In the rejections infra, reference labels are generally recited only for the first recitation of identical claim language.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5-9, 12-17, 84 and 85 are rejected under 35 U.S.C. 102(b) as being anticipated by Perkins (5239448).

At column 2, lines 29-39; column 3, line 45 to column 4, line 32; column 5, line 56 to column 6, line 21; and column 8, lines 4-16, Perkins teaches the following:

1. A semiconductor device comprising an interconnection board "locally complex area (MCM) and 2" having first and second surfaces (the second surface is the surface directly in contact with the plate 40); and a high rigidity plate 40 securely fixed to and directly in contact with at least a majority of said second surface of said interconnection board, said high

rigidity plate being higher in rigidity than said interconnection board for suppressing said interconnection board from being bent upon receipt of any stress applied during at least a process for manufacturing said interconnection board.

2. The semiconductor device as in 1, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure 2, 8, 12, 14, 18, 20, 24.

5. The semiconductor device as in 1, wherein said high rigidity plate is made of a ceramic.

6. The semiconductor device as in 1, wherein a base material of said interconnection board is an organic insulative material "polyimide."

7. The semiconductor device as in 6, wherein said organic material is a polymer resin material.

8. A semiconductor device comprising an interconnection board having first and second surfaces; at least one semiconductor chip 28 mounted on said first surface of said interconnection board; and a high rigidity plate securely fixed to and directly in contact with at least a majority of said second surface of said interconnection board, said high rigidity plate being higher in rigidity than said interconnection board for suppressing said interconnection board from being bent upon receipt of any stress applied during at least a process

for manufacturing said interconnection board, and for mounting said at least one semiconductor chip on said first surface.

9. The semiconductor device as in 8, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure.

12. The semiconductor device as in 8, wherein said high rigidity plate is made of a ceramic.

13. The semiconductor device as in 8, wherein a base material of said interconnection board is an organic material.

14. The semiconductor device as in 13, wherein said organic material is a polymer resin material.

15. The semiconductor device as in 8, wherein said at least semiconductor chip is indirectly bonded via bumps 30 to said second surface of said interconnection board.

16. The semiconductor device as in 15, wherein further comprising a sealing resin material 31 provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

17. The semiconductor device as in 16, further comprising at least a heat spreader 1 provided on said at least semiconductor chip.

84. The semiconductor device as in 1, wherein said high rigidity plate is securely fixed to and directly contact with an entirety of said second surface.

85. The semiconductor device as in 8, wherein said high rigidity plate is securely fixed to and directly contact with an entirety of said second surface.

To further clarify the teaching of a heat spreader 1, it is noted that a heat spreader is merely an element intended to be used for spreading heat, and this statement of intended use does not result in a structural difference between the claimed product and the product of Perkins. In fact, at column 4, lines 18-22, Perkins teaches that the plate 40 "can be used to provide thermal enhancement." Further, because the product of Perkins has the same structure as the claimed product, it is inherently capable of being used for the intended use, and the statement of intended use does not patentably distinguish the claimed product from the product of Perkins. Similarly, the manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perkins as applied to claims 1 and 8, and further in combination with Hurwitz (6280640).

Perkins does not appear to explicitly teach the following:

3. The semiconductor device as in 1, wherein said high rigidity plate is made of a metal.

10. The semiconductor device as in 8, wherein said high rigidity plate is made of a metal.

Nevertheless, as previously cited, Perkins teaches a ceramic plate, and at column 5, lines 26-37, Hurwitz teaches that metal and ceramic plates are equivalents; therefore, it would have been obvious to substitute the metal plate of Hurwitz for the ceramic plate of Perkins.

In any case, it would have been obvious to substitute the metal plate of Hurwitz for the ceramic plate of Perkins because it would provide a plate, and substitution of a known element based on its suitability for its intended use has been held to be prima facie obvious. See MPEP 2144.07.

Claims 1-3, 5-10, 12-15 and 80-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hurwitz (6280640), or in the alternative, over the combination of Hurwitz (6280640) and Perkins (5239448).

At column 4, lines 23-29, column 5, line 24 to column 6, line 31, column 7, lines 56-58, column 8, lines 32-37, column 9, lines 8-10, 30 and 48-52, and column 10, lines 7-9 and 30-33, Hurwitz teaches the following:

1. A semiconductor device comprising an interconnection board 18 having first and second surfaces; and a high rigidity (inherently high enough to maintain "high flatness") plate 12 securely fixed to and directly in contact with at least a majority of said second surface of said interconnection board, said high rigidity plate being equal in rigidity to said interconnection board for suppressing said interconnection board from being bent upon receipt of any stress applied during at least a process for manufacturing said interconnection board.

2. The semiconductor device as in 1, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure 14, 16.

3. The semiconductor device as in 1, wherein said high rigidity plate is made of a metal.

5. The semiconductor device as in 1, wherein said high rigidity plate is made of a ceramic.

6. The semiconductor device as in 1, wherein a base material of said interconnection board is an organic insulative material.

7. The semiconductor device as in 6, wherein said organic material is a polymer resin material.

8. A semiconductor device comprising an interconnection board having first and second surfaces; at least one semiconductor chip mounted on said first surface of said interconnection board; and a high rigidity plate securely fixed to and directly in contact with at least a majority of said second surface of said interconnection board, said high rigidity plate being equal in rigidity to said interconnection board for suppressing said interconnection board from being bent upon receipt of any stress applied during at least a process for manufacturing said interconnection board, and for mounting said at least one semiconductor chip on said first surface.

9. The semiconductor device as in 8, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure.

10. The semiconductor device as in 8, wherein said high rigidity plate is made of a metal.

12. The semiconductor device as in 8, wherein said high rigidity plate is made of a ceramic.

13. The semiconductor device as in 8, wherein a base material of said interconnection board is an organic material.

14. The semiconductor device as in 13, wherein said organic material is a polymer resin material.

15. The semiconductor device as in 8, wherein said at least semiconductor chip is indirectly bonded via bumps 19 to said second surface of said interconnection board.

80. A semiconductor device comprising: an interconnection board having first and second surfaces; at least one external electrode pad 20 buried in said interconnection board, said at least one external electrode pad having an exposed surface level with said second surface so that said second surface and said exposed surface form a single flat plane; and a high rigidity plate securely fixed to and directly contact with at least a majority of said single flat plane, said high rigidity plate being at least equal in rigidity to the interconnection board and suppressing said interconnection board from being bent.

81. The semiconductor device as in 80, wherein said high rigidity late is securely fixed to and directly in contact with an entirety of said single flat plane.

82. A semiconductor device comprising: an interconnection board having first and second surfaces; at least one external electrode pad buried in said

interconnection board, said at least one external electrode pad having an exposed surface level with said second surface so that said second surface and said exposed surface form a single flat plane; at least a semiconductor chip mounted on said first surface of said interconnection board; a high rigidity plate securely fixed to and directly in contact with at least a majority of said single flat plane, said high rigidity plate being equal in rigidity to said interconnection board and suppressing said interconnection board from being bent.

83. The semiconductor device as in 82, wherein said high rigidity plate is securely fixed to and directly contact with an entirety of said single flat plane.

84. The semiconductor device as in 1, wherein said high rigidity plate is securely fixed to and directly contact with said second surface.

85. The semiconductor device as in 8, wherein said high rigidity plate is securely fixed to and directly contact with an entirety of said second surface.

To further clarify the teaching of said high rigidity plate for suppressing said interconnection board from being bent upon receipt of any stress applied during at least a process for manufacturing said interconnection board, and for mounting said at least one semiconductor chip on said first surface, it is noted that this limitation is a statement of intended use of the product which does not result in a structural difference between the claimed

product and the product of Hurwitz. Further, because the product of Hurwitz has the same structure as the claimed product, it is inherently capable of being used for the intended use, and the statement of intended use does not patentably distinguish the claimed product from the product of Hurwitz. Similarly, the manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

However, Hurwitz does not appear to explicitly teach that the high rigidity plate is higher in rigidity than the interconnection board.

Regardless, as cited, Hurwitz teaches that the high rigidity plate is at least inherently equal in rigidity to the interconnection board (because they are coextensive and integral). Moreover, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative rigidity limitation because applicant has not disclosed that the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the process would possess utility using another rigidity. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809

(CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III), "Applicant can rebut a prima facie case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.' In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results."

In the alternative, as cited supra, Perkins teaches wherein a high rigidity plate 40 is higher in rigidity than an interconnection board "locally complex area (MCM)" for suppressing the interconnection board from being bent upon receipt of any stress applied during at least a process for manufacturing the interconnection board, and for mounting at least one semiconductor chip 28 on a first surface. In addition, it would have been obvious to combine the product of Perkins with the product of Hurwitz because, as taught by Perkins, it would suppress the interconnection board from being bent upon receipt of any stress applied during at least a process

for manufacturing the interconnection board, and for mounting at least one semiconductor chip on a first surface.

Moreover, it would have been obvious to substitute the board of Perkins for the board of Hurwitz because it would provide a board, and substitution of a known element based on its suitability for its intended use has been held to be prima facie obvious. See MPEP 2144.07.

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Hurwitz and Perkins as applied to claim 15.

Hurwitz does not appear to explicitly teach the following:

16. The semiconductor device as in 15, wherein further comprising a sealing resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

Still, as previously cited, Perkins teaches this limitation. Moreover, it would have been obvious to combine the teachings of Perkins and Hurwitz because it would relieve stress.

Also, at column 5, lines 18-21, and column 10, lines 16-18, Hurwitz teaches the following:

17. The semiconductor device as in 16, further comprising at least a heat spreader "structures" and "filled via structure" provided on said at least semiconductor chip.

Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perkins or Hurwitz or the combination of Hurwitz and Perkins as applied to claims 1 and 8, and further in combination with Farquhar (6329713).

Hurwitz and/or Perkins do not appear to explicitly teach the following:
4. The semiconductor device as in 1, wherein said high rigidity plate is made of an alloy.
11. The semiconductor device as in 8, wherein said high rigidity plate is made of an alloy.

Notwithstanding, at column 3, line 64 to column 4, line 1; and column 4, lines 36-67, Farquhar teaches wherein a high rigidity plate 8 is made of an alloy "Invar". Moreover, it would have been obvious to combine the product of Farquhar with the product of the applied prior art because it would provide the high rigidity plate of the prior art.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perkins or Hurwitz or the combination of Hurwitz and Perkins as applied to claims 16 and 17, and further in combination with Tsukamoto (5841194).

Although, as cited, Perkins and Hurwitz teach a heat spreader provided on said semiconductor chip, they do not teach the particular heat spreader 701 taught by Tsukamoto at column 4, line 59 to column 8, line 61. Nonetheless, it would have been obvious to combine the heat spreader of

Tsukamoto with the product of the applied prior art because it would improve thermal characteristics.

Claims 18-20, 27-37, 43, 44 and 50-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Allen (4705205) and Hayashi (JP11238972).

At column 1, line 10 to column 2, line 20; column 2, lines 46 to column 2, line 68; column 3, lines 42-49; column 4, lines 1-21; column 8, lines 32-40; column 8, lines 62-68; column 12, line 22 to column 13, line 46; column 13, line 66 to column 14, line 38; column 15, lines 8-45; column 16, lines 27-39; column 16, line 52 to column 17, line 18; column 18, lines 15-20; column 18, line 66 to column 19, line 16; column 20, lines 37-58; and column 21, lines 12-28, Allen teaches the following:

18. A semiconductor device comprising an interconnection board 32 having first and second surfaces; at least one external electrode pad 10 in said interconnection board, said at least one external electrode pad having an exposed surface; at least a semiconductor chip mounted on said interconnection board; and buffer layer means 20 having a first surface in contact with said second surface of said interconnection board and a second surface on which at least one external electrode 28 is provided, said buffer layer means for providing at least one electrical contact 28 between said one external electrode pad and said at least one external electrode and for

absorbing and/or relaxing a stress applied to said at least external electrode to make said interconnection board free from application of said stress.

20. The semiconductor device as in 18, wherein said at least external electrode comprises plural external electrodes.

27. The semiconductor device as in 18, wherein said buffer layer means comprises plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad 10 of said interconnection board and a second end directly fixed said external electrode.

28. The semiconductor device as in 27, wherein said plural generally column shaped electrically conductive layers are made of a metal.

29. The semiconductor device as in 18, wherein said buffer layer means comprises plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad of said interconnection board and a second end directly fixed said external electrode; and an stress absorption layer 22 filling gaps between said plural generally column shaped electrically conductive layers, and said stress absorption layer being lower in rigidity than said plural generally column shaped electrically conductive layers, and said stress absorption layer surrounding said plural generally column shaped electrically conductive

layers so that said stress absorption layer is in tightly contact with said plural generally column shaped electrically conductive layers.

30. The semiconductor device as in 29, wherein said plural generally column shaped electrically conductive layers are made of a metal.

31. The semiconductor device as in 29, wherein said stress absorption layer is made of an organic insulative material.

32. The semiconductor device as in 18, wherein said buffer layer means comprises plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad of said interconnection board and a second end directly fixed said external electrode; a supporting plate 22 having plural holes, into which said plural generally column shaped electrically conductive layers with said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said interconnection board to form an inter-space between said supporting plate and said second surface of said interconnection board ; and a supporting sealing resin material 22 filling said inter-space and surrounding both said plural generally column shaped electrically conductive layers and parts of said external electrodes so that said supporting sealing resin material is in tightly contact with said plural generally column shaped electrically conductive layers and said parts of said external electrodes for supporting said external electrodes.

33. The semiconductor device as in 32, wherein said supporting sealing resin material is lower in rigidity than said plural generally column shaped electrically conductive layers so that said supporting sealing resin material is capable of absorbing and/or relaxing a stress applied to said external electrodes.

34. The semiconductor device as in 32, wherein said plural generally column shaped electrically conductive layers are made of a metal.

35. The semiconductor device as in 32, wherein said supporting sealing resin material is made of an organic insulative material.

36. The semiconductor device as in 18, further comprising a supporting layer 34 on said second surface of said buffer layer means for supporting said external electrode.

37. The semiconductor device as in 36, wherein said supporting layer further comprises: a supporting plate 22 having plural holes into which holes said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said buffer layer means to form an inter-space between said supporting plate and said second surface of said buffer layer means; and a supporting sealing resin material 22 filling said inter-space and surrounding parts of said external electrodes so that said

supporting sealing resin material is in tight contact with said parts of said external electrodes for supporting said external electrodes.

43. A semiconductor device comprising an interconnection board having first and second surfaces; at least a semiconductor chip mounted on said interconnection board; at least one external electrode fixed to said at least one external electrode pad; a supporting layer 22 on said second surface of said interconnection board for supporting said external electrodes a buffer layer 20 having a first surface in contact with said second surface of said interconnection board, and wherein said supporting layer further comprises a supporting plate 22 having plural holes into which holes said external electrodes are inserted, and said supporting plate extending in parallel (at the surface of the supporting plate opposite the surface of the supporting plate coplanar with the first surface) to said second surface of said buffer layer to form an inter-space between said supporting plate (at the surface of the supporting plate opposite the surface of the supporting plate coplanar with the first surface) and said second surface of said buffer layer; and a supporting sealing resin material 22 filling said inter-space and surrounding parts of said external electrodes so that said supporting sealing resin material is in tight contact with said parts of said external electrodes for supporting said external electrodes.

50. The semiconductor device as in 43, wherein said external electrodes connected through plural generally column shaped electrically conductive layers to external electrode pads on said second surface of said interconnection board, and said supporting layer further comprises a supporting plate 22 having plural holes, into which said plural generally column shaped electrically conductive layers with said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said interconnection board to form an inter-space between said supporting plate and said second surface of said interconnection board; and a supporting sealing resin material 22 filling said inter-space and surrounding both said plural generally column shaped electrically conductive layers and parts of said external electrodes so that said supporting sealing resin material is in tightly contact with said plural generally column shaped electrically conductive layers and said parts of said external electrodes for supporting said external electrodes.

51. The semiconductor device as in 50, wherein said supporting sealing resin material is lower in rigidity than said plural generally column shaped electrically conductive layers so that said supporting sealing resin material is capable of absorbing and/or relaxing a stress applied to said external electrodes.

52. The semiconductor device as in 50, wherein said plural generally column shaped electrically conductive layers are made of a metal.

53. The semiconductor device as in 50, wherein said supporting sealing resin material is made of an organic insulative material.

However, Allen does not appear to explicitly teach the external electrode pad buried in the interconnection board, and having the exposed surface level with the second surface so that the second surface and the exposed surface form a single flat plane, or the following:

19. The semiconductor device as in 18, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure.

Nonetheless, in the English abstracts and figures, Hayashi teaches an external electrode pad 2 buried in an interconnection board 1, and having the exposed surface level with a second surface so that the second surface and the exposed surface form a single flat plane, wherein the interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure. Furthermore, it would have been obvious to combine the product of Hayashi with the product of Allen because it would provide an interconnection board.

Claims 21, 38-42, 45-49 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Allen and Hayashi as applied

to claims 18-20, 27-37, 43, 44 and 50-53, and further in combination with Tsukamoto.

The combination of Allen and Hayashi does not appear to explicitly teach the following:

21. The semiconductor device as in 18, wherein said external electrode comprises a solder ball.

38. The semiconductor device as in 18, wherein said at least semiconductor chip is bonded via bumps to said first surface of said interconnection board.

39. The semiconductor device as in 38, wherein further comprising a sealing resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

40. The semiconductor device as in 39, further comprising at least a heat spreader provided on said at least semiconductor chip.

41. The semiconductor device as in 38, wherein further comprising an under-fill resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

42. The semiconductor device as in 41, further comprising a stiffener extending on a peripheral region of said buffer layer means; and at least a heat spreader provided on said at least semiconductor chip and on said stiffener.

45. The semiconductor device as in 43, wherein said at least semiconductor chip is bonded via bumps to said first surface of said interconnection board.
46. The semiconductor device as in 45, wherein further comprising a sealing resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.
47. The semiconductor device as in 46, further comprising at least a heat spreader provided on said at least semiconductor chip.
48. The semiconductor device as in 45, wherein further comprising an under-fill resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.
49. The semiconductor device as in 48, further comprising: a stiffener extending on a peripheral region of said buffer layer; and at least a heat spreader provided on said at least semiconductor chip and on said stiffener.
54. The semiconductor device as in 43, wherein said external electrode comprises a solder ball.

Nonetheless, at column 4, line 59 to column 8, line 61, Tsukamoto teaches a semiconductor device wherein an external electrode comprises a solder ball, a semiconductor chip 201 is bonded via bumps 204 to a first surface of an interconnection board 101, a sealing resin 205 material provided on the first surface of the interconnection board for sealing the semiconductor chip and the bumps, an under-fill resin material 205 provided

on the first surface of the interconnection board for sealing the at least semiconductor chip and the bumps, a stiffener 106 extending on a peripheral region of the interconnection board; and at least a heat spreader 701 provided on the semiconductor chip and on the stiffener. Moreover, it would have been obvious to combine the product of Tsukamoto with the product of the applied prior art because it would provide a chip carrier having improved manufacturing yield.

Applicant's amendment and remarks filed 9-2-3 have been fully considered, are addressed by the rejections supra, and are further addressed infra.

Applicant argues that Hurwitz does not teach that the base is at least inherently equal in rigidity to the board because, allegedly, "joining of two materials does not change the rigidity of either, it establishes the rigidity of the combination."

This argument is respectfully traversed because, when rigidity is defined as the quality or state of having the outer shape maintained by a fixed framework; for example, the fabric envelope outer shape of an airship maintained by the airship fixed framework, the joining of the two materials of the fabric envelope and the framework changes the rigidity of the fabric envelope.

This argument is further deemed unpersuasive because it does not preclude that the alleged established rigidity of the combination is equal to the rigidity of the base and the board. In fact, it is precisely the inherent establishment of a rigidity of the combination of the base and the board that lends equal rigidity to the base and the board.

Applicant also asserts that, "rigidity is a function of dimensions of the material . . . One of skill in the art would not make any evaluation of the rigidity of the base relative to the rigidity of the board structure . . . because there is not sufficient information to do so."

This assertion is respectfully deemed unpersuasive because there is no art recognized definition of rigidity as a function of dimensions of a material, and this function is not otherwise defined in the disclosure. Similarly, there is no art recognized information sufficient to make an evaluation of the rigidity of the base relative to the board, and this information is not otherwise defined in the disclosure.

To this end, applicant and the assignee of this application are required under 37 CFR 1.105 to provide the following information that the examiner has determined is reasonably necessary to the examination of this application.

Specifically, applicant is required to provide the referenced function of dimensions of a material which is rigidity, and the referenced information

sufficient to make an evaluation of the rigidity of the base relative to the board.

Also, in response to this requirement, please state the specific improvements of the subject matter in claims the claims having the "rigidity" limitation over the disclosed prior art and indicate the specific elements in the claimed subject matter that provide those improvements. For those claims expressed as means or steps plus function, please provide the specific page and line numbers within the disclosure which describe the claimed structure and acts.

Applicant is reminded that the reply to this requirement must be made with candor and good faith under 37 CFR 1.56. Where applicant does not have or cannot readily obtain an item of required information, a statement that the item is unknown or cannot be readily obtained will be accepted as a complete reply to the requirement for that item.

A complete reply to this Office action must include a complete reply to the requirement for information. The time period for reply to the requirement coincides with the time period for reply to this Office action.

Applicant also contends that the instant invention produces unexpected results because, "None of this can be inferred from the applied references and thus the results are unexpected."

This contention is respectfully deemed unpersuasive because the alleged inability to infer the alleged results from the applied prior art is not evidence of unexpected results.

Applicant additionally argues that there is no motivation to combine Hurwitz and Perkins.

This argument is respectfully traversed because motivation to combine is explicitly and clearly provided; namely, "it would have been obvious to combine the product of Perkins with the product of Hurwitz because, as taught by Perkins, it would suppress the interconnection board from being bent upon receipt of any stress applied during at least a process for manufacturing the interconnection board, and for mounting at least one semiconductor chip on a first surface." Indeed, this is exactly the purpose of the board of the instant invention.

Relatedly, applicant proffers that there is no motivation to combine the board of Perkins with the teaching of Hurwitz because, "the HURWITZ et al. device already has a base 12 that is used for a particular purpose."

This proffer is respectfully deemed unpersuasive because the motivation to combine is predicated on a different purpose than the alleged particular purpose. In any case, as recited in the rejection, substitution of a known element based on its suitability for its intended use has been held to be prima facie obvious. See MPEP 2144.07.

Applicant also argues that the applied prior art does not teach the claim 18 "means for" limitation because, allegedly, the interpretation of the limitation is governed by 35 U.S.C. 112, sixth paragraph.

This argument is respectfully traversed for the reasons stated in the 35 U.S.C. 112, second paragraph rejection supra. In addition, in the claims, the phrase "means for" is modified by sufficient structure, material or acts for achieving the specified function; therefore, the USPTO will not apply 35 U.S.C. 112, sixth paragraph until such modifying language is deleted from the claims. See MPEP 2181.

Applicant also asserts that the prior art does not teach "the separate supporting plate and buffer layer now claimed [in claim 43]."

This assertion is respectfully deemed unpersuasive for the reasons stated in the rejection supra, and because the scope of claim 43 is not limited to a separate supporting plate and buffer layer. Hence, the prior art is not necessarily applied to the rejection for this teaching.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947, or after about 02/05/04, (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
11-Dec-03